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8.3.2 A MICROPROGRAMMABLE RADAR CONTROLLER

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The Wave Propagation Laboratory has completed the design and construction of a microprogrammable radar controller for atmospheric wind profiling. Unlike some radar controllers using state machines or hardwired logic for radar timing, this design is a high speed programmable sequencer with signal processing resources. A block diagram of the device is shown in Figure 1.

The device is a single 8 1/2" x 10 1/2" printed circuit board and consists of three main subsections: 1) the host computer interface, 2) the microprogram sequencer, and 3) the signal processing circuitry.

HOST INTERFACE

The host computer bus chosen for this design is the Digital Equipment Corporation Q-Bus supported by DEC's 11/23, 11/73, and MicroVAX computers.

The radar interface control/status register (RICSR) allows control of the radar controller from the host. The RF control/status register (RFCSR) allows the host to control the operation and check the status of up to seven external RF devices such as the receiver/exciter, the antenna controller, the pulse amplifier, etc.

MICROPROGRAM SEQUENCER

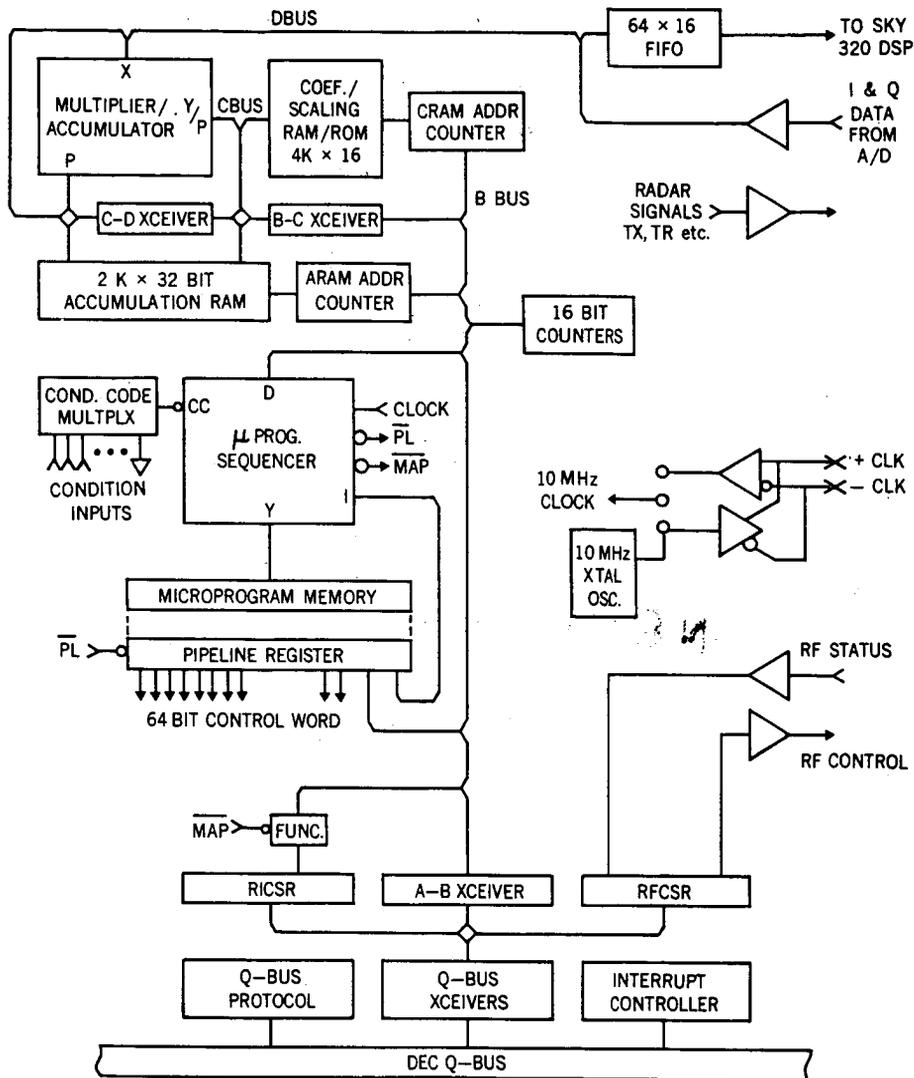
An Advanced Micro Devices 2910A microprogram sequencer determines the address for the microprogram memory. Such features as an internal loop counter, a 9-word deep stack for microsubroutines, and condition testing allows efficient microcoding for radar control and signal processing. The microprogram memory is 2048 words deep by 64 bits wide. Most of the bits in the microword control the microprogram sequencer and the signal processor but eight of these bits are sent out for high speed radar timing signals such as Transmit, T/R, Receiver Blank, A/D Sample, Pulse Coding, etc. Since the sequencer runs at 10 MHz, these signals are all controllable with 100 nanosecond resolution. The clock source may either be an on-board crystal oscillator or a 10-MHz external reference oscillator such as the master oscillator in a phase locked receiver design.

SIGNAL PROCESSING

In-phase (I) and Quadrature (Q) digital data are sequentially processed using a high speed 16 x 16 bit multiplier-accumulator and a 2048-word deep by 32-bit wide accumulation memory.

If simple time-domain averaging is desired, the coefficient/scaling memory contains a fixed scale factor which, when multiplied by each incoming sample and accumulated without truncation, results in a properly scaled value in the most significant 16 bits of the accumulation memory at the end of the time-domain averaging period.

A weighted average may be implemented by multiplying each incoming sample by a weighting value from the coefficient/scaling memory along with the



**RADAR CONTROLLER
BLOCK DIAGRAM**

Figure 1.

accumulation. This is a digital transverse low pass filter and has been used to help reject RF interference and moving targets.

After the averaging process, the data are sent out of the device via the First In-First Out memory to a commercially available digital signal processing board. The SKY320, manufactured by Sky Computers, Inc., sorts the data, performs dc removal, performs the fast Fourier transform, and the windows the spectra. The SKY320 is programmed to process 128 point complex time series from 36 range gates and is operating at one-third its maximum throughput capacity.

Data are then retrieved from the SKY320 by the host computer which performs spectral moment calculation, wind calculations, etc.

This configuration results in real-time operation (100% dwell time) without the use of expensive array processors or high speed memory.

MICROCODE DEVELOPMENT

Microcode is written on the host machine using commercial meta assembler software. An auxiliary writable control-store board substitutes for the Radar Controller microprogram memory during development. Programmable Read Only Memory is then loaded with the developed microcode and is used as the microprogram memory for a fixed number of radar parameters.

A NOAA Technical Memorandum detailing the design and microprogramming of the device is planned for 1986.